Lab for High Performance Computing
Department of Computer Science and Automation
Convenor: Prof. R. Govindarajan

**Memory Hierarchy**
- Micro-architecture
- General Purpose
- Application Specific
- Embedded Systems

**Network Processors**
- Network Processor Architecture
- Network Processor Architecture

**Programmability**
- Performance
- Power Efficiency

**HPC**
- Compiler Optimizations
- Compiler Analysis
- Research Funding
- AMD, DST, IBM, Intel, Microsoft, NVIDIA

**COMPILETORS**
- Compiler Optimizations
- Compiler Analysis

**Cache Placement & Replacement Policies**
- Improving cache hit rates using next-use distance estimates
- Adaptive cache placement to reduce conflict misses
- Two-level mapping based placement
- Emulating the optimal placement policy with a shepherd cache

**Prefetching**
- Estimation of prefetch history effectiveness using entropy
- Identifying and eliminating misses that cause pipeline stalls

**Power Performance Efficient Architectures**
- Segmented low power issue queues
- Scalable energy efficient store queues
- Heterogeneous width register files for superscalar architectures

**Software Transactional Memory**
- Compiler transformations to improve cache performance
- Compiler transformations to reduce number of conflicts

**Distributed Shared Memory**
- Compiler and software assisted distributed shared memory (DSM)

**Clusters**
- Cluster based web servers
- Cache performance for web server architectures
- Exploiting communication processors for improving application performance

**Compiler Optimizations**
- Code size aware instruction scheduling
- Energy aware compilation techniques, exploiting DVFS
- Energy aware instruction scheduling and S/W pipelining

**Compiler Analysis**
- Scalable context-sensitive points-to analysis through randomization
- Points-to analysis as a system of linear equations
- Comprehensive path-sensitive data flow analysis

**Over 75 Publications**
- 2 Best Thesis Awards
- 2 Best Paper Awards

**Students**: Graduated (Current)
- ME/MTech: 13 (0)
- MSc(Engg): 16 (2)
- PhD: 3 (5)

**Memory Arch. Exploration**
- Evolutionary approach for memory architecture exploration
- Integration of architecture and data layout exploration
- Pareto optimal design points for power, performance and cost
- Hybrid memory architectures involving cache and scratchpads

**Research Funding**
- AMD, DST, IBM, Intel, Microsoft, NVIDIA

**http://hpc.serc.iisc.ernet.in**